DATE: August 16, 2010   **PAGES** (+COVER): 4

FROM: Patrick D. Reed	**TO:** Ben C. Wang
PHONE: 509-944-4752	**PHONE:** 571-270-1240
FAX #: 509-323-8979	**FAX #:** 571-270-2240

lee&hayes

RE: 10/816,558   -Interview Request From

COMMENTS:

Hello Examiner Wang,

Please confirm receipt of fax and acceptance of interview.

I look forward to working with you on this matter.

Regards,

Patrick

thanks

Attorney Docket   MS1 - 4217US

lee & hayes pllc, intersection of ip & business law

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Applicant Initiated Interview Request Form

Application No.: ___10/816,558___ First Named Applicant:_Lucius Gregory Meredith_

Examiner: _Ben C. Wang_ Art Unit: _2192_ Status of Application: _Non-Final_

Tentative Participants:

(1) _Ben C. Wang_ (2) _Patrick D. Reed_

(3) _____ (4) _____

Proposed Date of Interview: _Thurs, August 19, 2010_ Proposed Time: _1:30pm EDT_ AM/**PM**

Type of Interview Requested:

(1) ☑ Telephonic (2) ☐ Personal (3) ☐ Video Conference

Exhibit To Be Shown or Demonstrated: ☐ YES ☐ NO

If yes, provide brief description: _____

Issues To Be Discussed

Issues (Rej., Obj., etc)	Claims/ Fig. #s	Prior Art	Discussed	Agreed	Not Agreed
(1) 103 Rej.	6, 42	Leach, Meredith	☐	☐	☐
(2)			☐	☐	☐
(3)			☐	☐	☐
(4)			☐	☐	☐

☐ Continuation Sheet Attached

Brief Description of Argument to be Presented:

1) Distinguishing the claims from the cited references in light of the proposed amendments.

_____

_____

An interview was conducted on the above-identified application on _____ .

NOTE: This form should be completed by applicant and submitted to the examiner in advance of the interview (see MPEP § 713.01).

This application will not be delayed from issue because of applicant's failure to submit a written record of this interview. Therefore, applicant is advised to file a statement of the substance of this interview (37 CFR 1.133(b)) as soon as possible.

Applicant/Applicant's Representative Signature	Examiner/SPE Signature
Patrick D. Reed	
Typed/Printed Name of Applicant or Representative	
61227	Attorney Docket MS1 -4217US
Registration Number, if applicable	

Unofficial Communication – For Discussion Purposes Only
Application No. 10/816,558

6.   (Proposed Amendments) A microprocessor for executing instructions, comprising:

a timing and control unit ~~for retrieving~~ <u>configured to:</u>

<u>retrieve</u> an instruction <u>to compose a plurality of processes running in parallel</u> from <u>a</u> memory, <u>the instruction being expressed in a reflective process algebra, the reflective process algebra being arranged to represent a name as a literalization of a process and a process as a deliteralization of a name,</u>

~~decoding~~ <u>decode</u> the instruction,

~~fetching~~ <u>fetch</u> data connected with the instruction, <u>the data comprising at least a first name that is a literalization of a first process and a second name that is a literalization of a second process, the first name and the second name being obtained using the reflective process algebra,</u> and

~~saving the~~ <u>literalize a</u> result <u>of a composing, including saving the result of the composing</u> ~~the data including names obtained by literalizing processes in a reflective process algebra~~; and

an arithmetic and logic unit ~~for performing an operation specified by the instruction~~ <u>configured to perform the composing of the plurality of processes running in parallel, the composing including deliteralizing the first name and the second name</u> ~~the instruction being expressed in a reflective process algebra, the reflective process algebra being capable of representing names as literalization of processes and processes as deliteralization of names~~.

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45.　(Proposed Amendments) An array of microprocessors for executing instructions, comprising:

at least one microprocessor that includes one or more components that are synchronized based on a program compiler configured to compile a program written in a reflective process algebra:

a timing and control unit for retrieving an instruction from memory, decoding the instruction, fetching data connected with the instruction, and saving [[the]] a result, the data including names obtained by literalizing processes in the reflective process algebra; and

an arithmetic and logic unit for performing an operation specified by the instruction, the instruction being expressed in [[a]] the reflective process algebra, the reflective process algebra being capable of representing names as literalization of processes and processes as deliteralization of names.

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